Docket No.: 8733.345.10
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Woo-Hyuk CHOI	Customer No.: 30827
Application No.: 10/774,517	Confirmation No. 8692
Filed: February 10, 2004	Art Unit: 2871
For: A METHOD OF MANUFACTURING AN ARRAY SUBSTRATE FOR USE IN A LCD DEVICE	Examiner: Dung T. Nguyen

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF CONFERENCE REQUEST

Sir:

Applicants request review of the final rejection of June 24, 2009, in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal.

In the Office Action, claims 11-14 and 16-21 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,166,085 to Wakai et al. (hereinafter "*Wakai*") in view of U.S. Patent No. 5,920,082 to Kitazawa et al. (hereinafter "*Kitazawa*") and U.S. Patent No. 6,288,414 to Ahn (hereinafter "*Ahn*"). *Office Action* at p. 2. Reconsideration and withdrawal of the rejection are requested.

Independent claim 11 is allowable over the cited references in that claim 11 recites a combination of elements for a method of fabricating a thin film transistor substrate that comprises, for example, "forming a gate pad electrode and a data pad electrode electrically contacting the gate pad and the data pad, respectively, wherein the at least one of the gate pad electrode and the data pad electrode is formed using the back exposure light of which passes

through the pad hole, wherein a region where the pad hole is formed is within a region where the contact hole is formed, and wherein the at least one of the gate pad electrode and the data pad electrode is within the region where the contact hole is formed". The cited references, analyzed alone or in any combination, do not teach or suggest at least these features of the claimed invention.

As admitted by the Office, *Wakai* "neither disclose the step of forming the pixel electrode by using a back exposure nor the step of forming a gate pad, a gate pad electrode as well as a data pad and a data pad electrode having pad holes therein." *Office Action* at p. 3. Thus, *Wakai* does not teach or suggest all of the features of independent claim 11.

The Office purports that "although *Ahn* does not explicitly disclose the back exposure light method for forming the gate/data pad electrode(s), *Kitazawa* ... disclose[s] a method of using a back exposure light for etching a layer over a substrate forming gate/data pad electrode ... and it is an evidence that one of ordinary skill in the art would be able to merely find how to apply a back exposure method for forming gate/data pad electrodes in a display device." *Office Action* at pp. 3-4. Applicants respectfully disagree.

Applicants submit that the Examiner appears to have made a clear error in modifying *Ahn's* disclosure of "gate/data pad electrodes connected to a gate/data line" with *Kitazawa's* purported disclosure of "using a back exposure light for etching a layer over a substrate forming gate/data pad electrodes." *Office Action* at p. 3. For reasons stated below, *Ahn's* gate pad electrode and data pad electrode cannot be "formed using the back exposure of light of which passes through the pad hole" because back light can not pass through *Ahn's* low resistance gate pad. Therefore, the combination of *Ahn* and *Kitazawa* to disclose the features of claim 11, as suggested by the Examiner, is improper and a clear error.

Ahn discloses that "[t]he aluminum layer is patterned to form ... a low resistance gate pad 117a" and "[t]he second metal layer is patterned to form ... a second-metal gate pad 117." *Ahn* at col. 5:27-30 and lines 33-36. *Ahn* discloses that a "protection layer 139 is patterned to form ... a gate pad contact hole 187" where "[t]he gate pad contact hole 187 exposes the second-metal gate pad 117 by removing the protection layer 139 and the gate insulation layer 119 covering the second-metal gate pad 117." *Ahn* at col. 6:7-11. In other words, the second-metal pad 117 is etched to form the gate pad contact hole 187, the low resistance gate pad 117a, however, is not etched and has no hole therein. The etching of the second-metal gate pad 117 is to remove a thin

second-metal oxide or nitride layer such that "the contact resistance between the pad and a pad terminal is reduced and the adhesion between them is enhanced." *Ahn* at col. 8:4-5. Therefore, *Ahn's* second-metal gate pad 117 is etched to from the gate pad contact hole 187 and the low resistance gate pad 117a remains without etching. Furthermore, the low resistance gate pad 117a is made of aluminum which is generally reflective and not transparent. Accordingly, any back light for forming the gate pad terminal 165 could not pass through the low resistance gate pad 117a. Therefore, *Ahn* cannot be modified with the back exposure method to form the gate pad terminal 165 as asserted by the Office.

Also, *Ahn* discloses that "[a]n indium tin oxide layer is deposited on the substrate 111 ... and is patterned to form ... a gate pad terminal 165." *Ahn* col. 6:18-20 and Figs 4e and 4d. As shown, *Ahn's* gate pad terminal 165 is formed within and outside of the region of the gate pad contact hole 187. Accordingly, *Ahn* fails to teach or suggest, "forming a gate pad electrode and a data pad electrode electrically contacting the gate pad and the data pad, respectively, wherein the at least one of the gate pad electrode and the data pad electrode is formed using the back exposure light of which passes through the pad hole, wherein a region where the pad hole is formed is within a region where the contact hole is formed, and wherein the at least one of the gate pad electrode and the data pad electrode is within the region where the contact hole is formed," as recited in independent claim 11.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the

filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to Deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: October 23, 2009

Respectfully submitted,

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